CTμL 9957•9967
FLIP-FLOPS
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS
+15°C TO +55°C TEMPERATURE RANGE

CTμL 9967 FLIP-FLOP GENERAL DESCRIPTION

The CTμL 9967 dual rank J-K Flip-Flop is a high speed directly coupled multi-purpose storage element useful for shift registers, counters, and other control functions.

Operation of the CTμL 9967 is based on the "master-slave" principle whereby information is entered into the "master" when the clock pulse goes high and is transferred to "slave" and outputs when the clock pulse goes low. DC coupling throughout makes the Flip-Flop input insensitive to rise and fall times.

The CTμL 9967 employs the PNP-NPN complementary logic to achieve fast response with typical toggling rate of 35 MHz. The emitter follower outputs are compatible with all other elements in the CTμL family.

Two phase clock outputs at half the clock input frequency is available when the CTμL 9967 is operated as a binary counter. Typical power dissipation is 420 mW and is designed to increase with fanout.

CTμL 9957 GENERAL DESCRIPTION

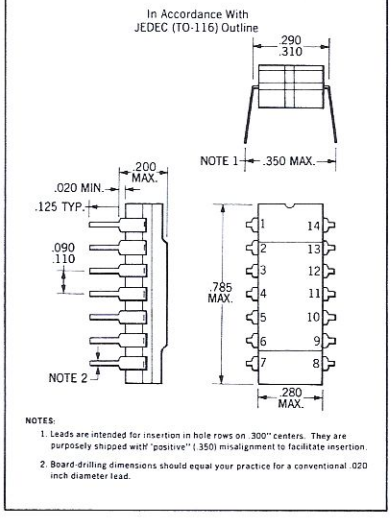
The CTμL 9957 is a basic dual-rank R-S Flip-Flop intended for storage and control function. Logic and clock inputs are omitted for additional flexibility. J-K operation with either two-phase or single-phase clocking can be exercised by adding AND-OR gates to the inputs. Wired OR ties within the flip-flop reduce typical through propagation delays to 14 ns.

The CTμL 9957 is DC coupled throughout. The inputs respond exclusively to voltage levels and are insensitive to rise and fall times. Emitter follower outputs, compatible with all other CTμL elements, provide efficient drive capability into long line and capacitive loads.

The CTμL 9967 and CTμL 9957 are packaged in the versatile Dual In-Line Package which is hermetically sealed ceramic package intended for low cost insertion techniques.

Both flip-flops are designed to operate over a commercial ambient temperature range of +15°C to +55°C. Power supplies are 4.5 volts ±10% and −2 volts ±10%.

PHYSICAL DIMENSIONS
TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION

DESCRIPTION	CODE	MARKING
CTμL 9957	U6A995779X	CTμL 95759
CTμL 9967	U6A996779X	CTμL 96779

Use the ten letter code for ordering purposes.
All units marked as above unless otherwise specified.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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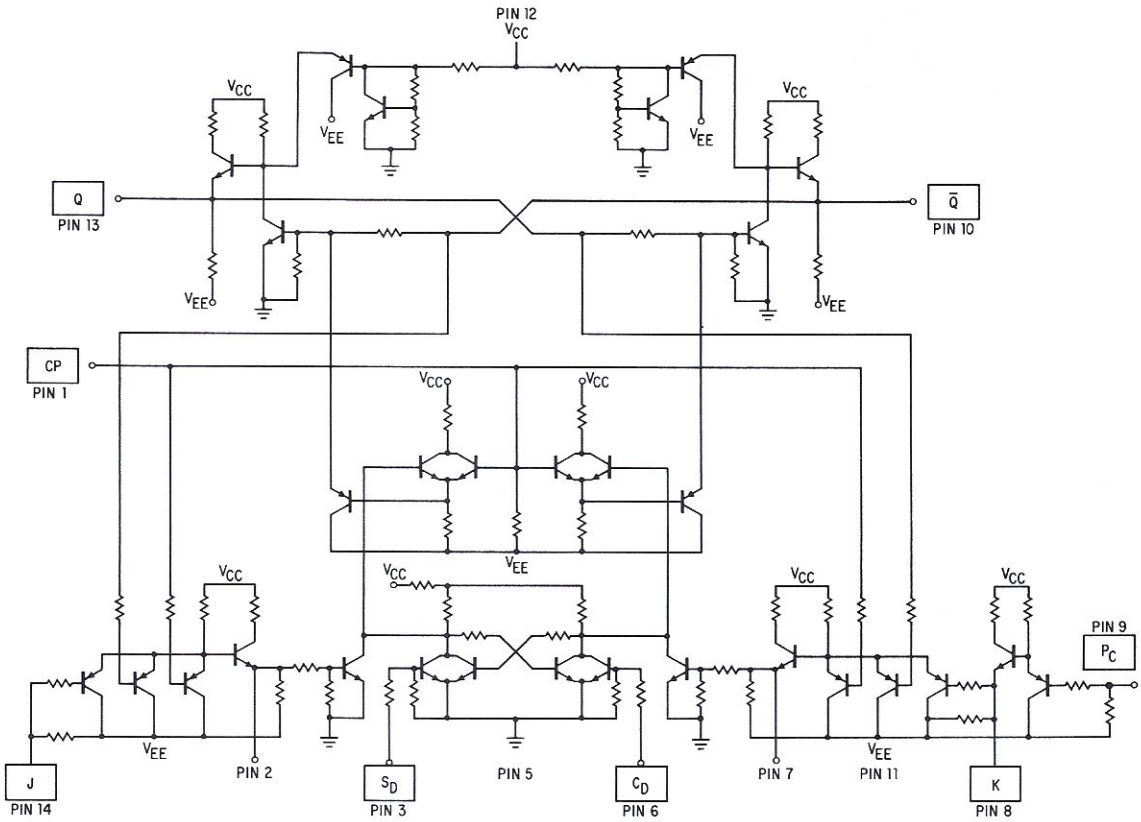
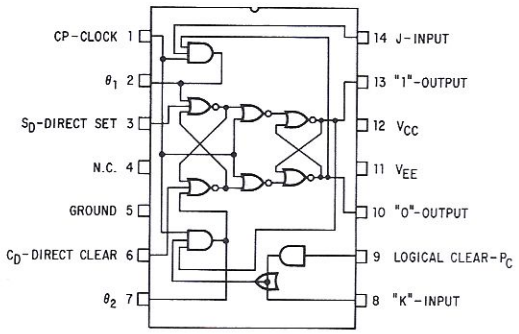
CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



PIN & LOGIC DIAGRAM CTμL9967 - JK FLIP FLOP



V_{CC} = 4.50 V
V_{EE} = −2.00 V
N.C. = NOT CONNECTED

TRUTH TABLE

SYNCHRONOUS ENTRY					ASYNCHRONOUS ENTRY			
		t_n		$t_n + 1$	Inputs		Outputs	
J	K	SD	CD	output (Q)	SD	CD	"1"	"0"
L	L	L	L	Q_n	L	L	NC	NC
L	H	L	L	L	L	H	L	H
H	L	L	L	H	H	L	H	L
H	H	L	L	$\bar{Q}_n$	H	H	H	H
L	L	L	H	H	Clock Input Low			
L	L	H	L	L				
L	L	H	H	Undetermined				

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP	2.0
J, K	1.0
S_D, C_D,	1.5
P_C	1.0
OUTPUTS	**FAN OUT**
Q, Q	12

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	−4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

ELECTRICAL CHARACTERISTICS

9967 DC TESTS

TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.[5]	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output	2.35	2.50		Volts	4.05	NOTE 1	[3]F.O. = 12	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested direct input to 3.50 V; tested direct input to 1.25 V; clock input to −0.70 V.
ONE Level Output			3.20	Volts	4.95	−1.80	F.O. = 1	Corresponding direct input is 3.50 V.
ZERO Level Output		−0.50	−0.36	Volts	NOTE 2	−1.80	F.O. = 1	Direct input to 3.50 V; other direct input to 0.80 V; logic inputs to 3.50 V; clock input to 0.47 V.
ONE Level Offset		200	270	mV	4.05	−2.20	F.O. = 4	Trigger and logic inputs sequentially to 2.25 V; untested inputs and outputs to 3.50 V.
ZERO Level Offset		120	195	mV	4.95	−1.80	F.O. = 1	Clock and logic inputs sequentially to −0.36 V. Untested inputs and outputs to 3.50 V.
Logic Input Pull-down Resistor	1.6 k	2.0 k	2.4 k	Ω	NOTE 2	−1.80	No Load	Logic input is 3.50 V.
Clock Input Pull-down Resistor	0.8 k	1.0 k	1.2 k	Ω	NOTE 2	−1.80	No Load	Clock input to 3.50 V.
Input Current		6.1	7.67	mA	NOTE 2	−1.80	No Load	Terminals 2 and 7 to 3.50 V.
Input Current		2.0	3.27	mA	4.05	−1.80	No Load	Direct set and clear inputs to 3.50 V.
Positive Supply Current		51.0	64.0	mA	4.95	−2.20	No Load	Clock input to −0.47 V.
Negative Supply Current		55.0	68.7	mA	4.95	−2.20	No Load	Clock, logic inputs and "1" outputs to 3.50 V simultaneously.
Clock Pulse Width - t_{PW}	25	16.0		ns	4.50	−2.00	F.O. = 12	Min. required pulse width to trigger 967.
Output Rising Delay - t_{dr}		10.0	15.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Output Falling Delay - t_{df}		16.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Direct Through Rising Delay - t_{sr}		17.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5
Direct Through Falling Delay - t_{sf}		25.0	38.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5

NOTES:

(1) Value of V_{EE} non-critical, $-1.80\ V \leq V_{EE} < -2.20\ V$.

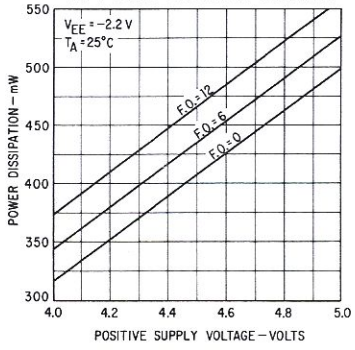
(2) Value of V_{CC} non-critical, $4.05\ V \leq V_{CC} \leq 4.95\ V$.

(3) F.O. = Fan-Out: F.O. = 12 equivalent to 133Ω to −2.20 V under worst case conditions.
F.O. = 4 equivalent to 400Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions.

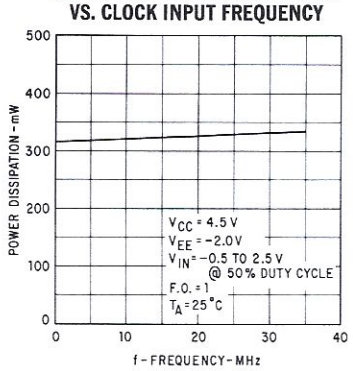
(4) Pulse is a positive pulse of non-critical amplitude and width.

(5) "Maximum" means "no more positive than."

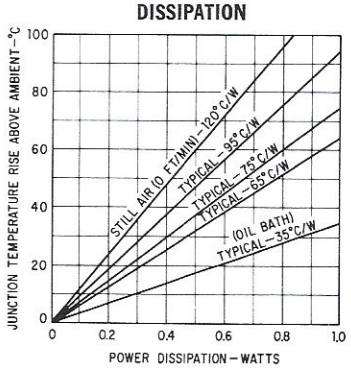
WORST CASE POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE



WORST CASE POWER DISSIPATION VS. CLOCK INPUT FREQUENCY



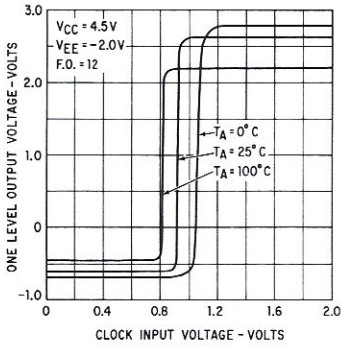
WORST CASE JUNCTION TEMPERATURE VS. POWER DISSIPATION



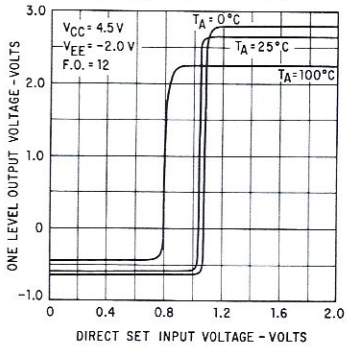
CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

TRANSFER CHARACTERISTICS

CLOCK-ONE LEVEL VERSUS TEMPERATURE

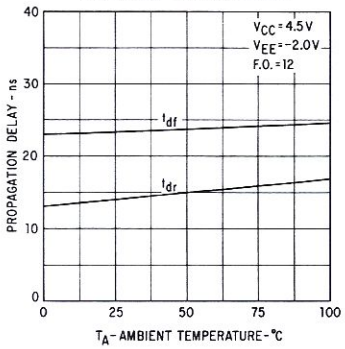


DIRECT SET/DIRECT CLEAR VERSUS TEMPERATURE

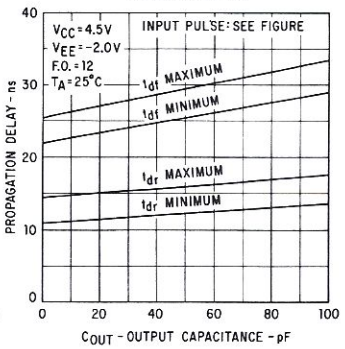


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

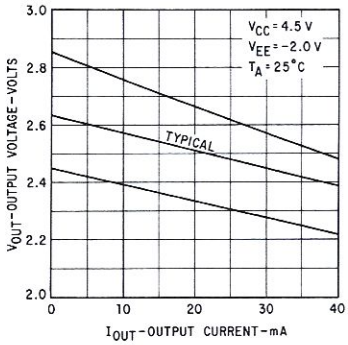


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

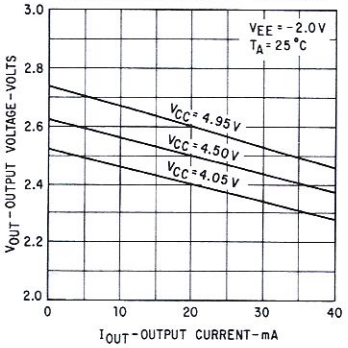


OUTPUT CHARACTERISTICS

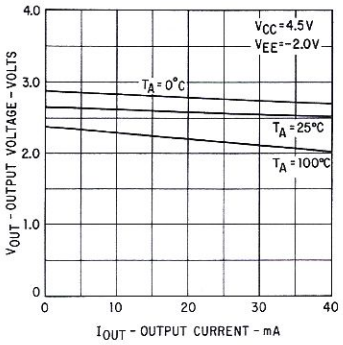
TOLERANCE VARIATION OF PARAMETERS



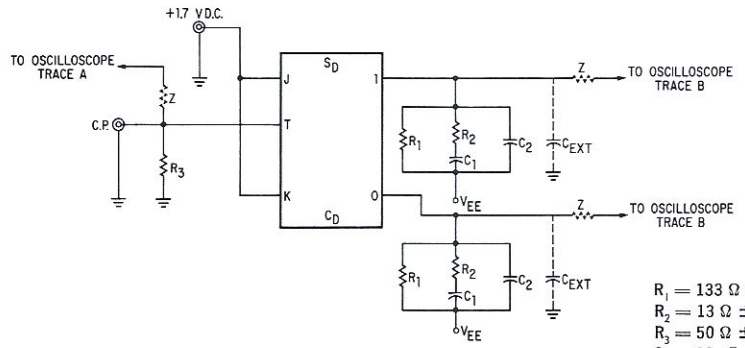
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



AS A FUNCTION OF TEMPERATURE



t_{df} and t_{dr} SWITCHING TIME TEST CIRCUIT



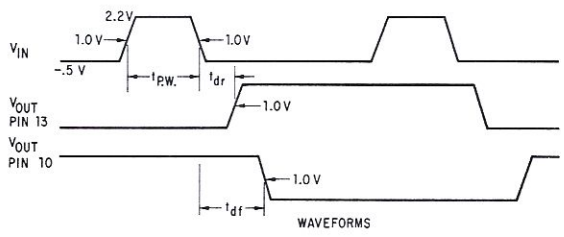
$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance ≥ 5k

SWITCHING NOTES:

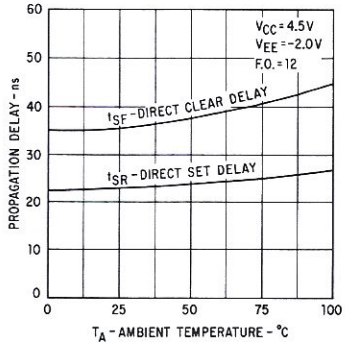
(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width (t_{PW}) = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

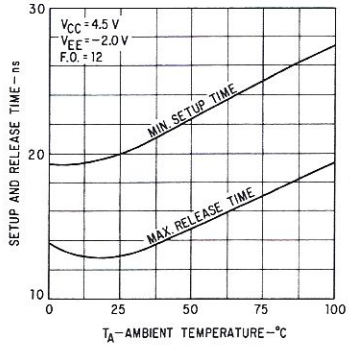
(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V



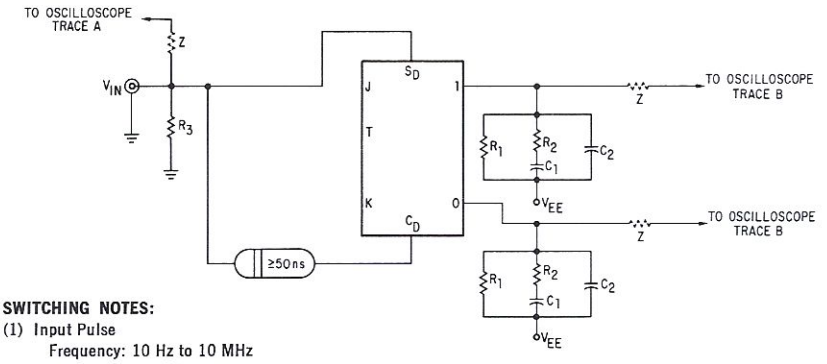
DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY VERSUS TEMPERATURE



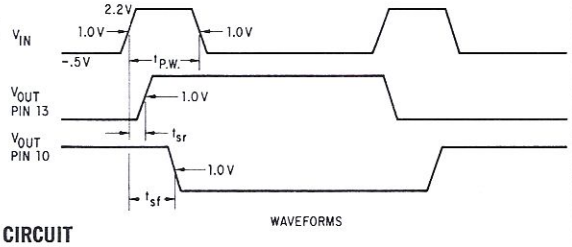
WORST CASE SETUP AND RELEASE TIME VERSUS TEMPERATURE



DIRECT SET & DIRECT CLEAR SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance $\geq$ 5k



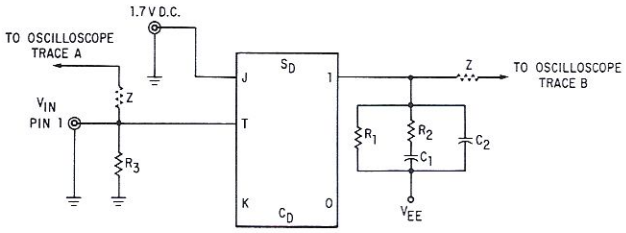
SWITCHING NOTES:

(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V

$t_{SET\text{-}UP}$ & $t_{RELEASE}$ SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance $\geq$ 5k

SWITCHING NOTES:

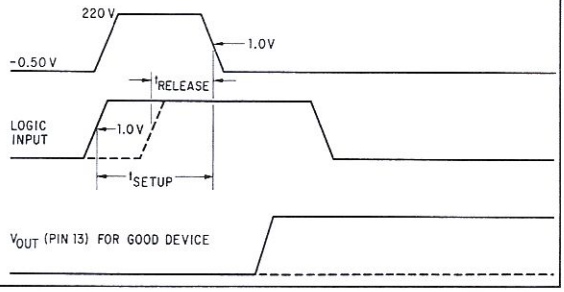
(1) Input Pulse
Rise Time = 10 ns
Fall Time = 10 ns
Amplitude = 2.10 V
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and the jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V.

(4) Similar tests may be made at "0" output if logic input is the "K" input.

(5) $t_{SET\text{-}UP}$ is defined as the minimum time required for a "ONE" to be present at either logic input prior to a clock transition from a high to a low in order for the flip-flop to respond. $t_{RELEASE}$ is defined as the maximum time required for a ONE to be present at either logic input prior to clock transition from a high to a low in order for the flip-flop not to respond.

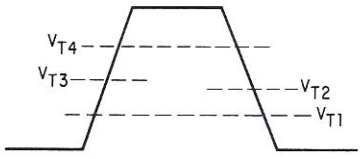


OPERATION OF FLIP-FLOP

The CTμL 9967 is directly coupled throughout and hence, its inputs are not sensitive to rise times. It responds exclusively to input voltage levels with definite, separated thresholds for both high and low voltage levels.

As the clock input rises from ZERO level, above V_{T1}, the transfer gates between the master and the slave are inhibited and the slave is isolated from the master. Above V_{T3}, the logic input gates are enabled and the master is set. Above V_{T4}, the master is sure to be set under the worst case condition and clock input is reaching the ONE level. As the clock input falls from the ONE level below V_{T4}, it inhibits the logic input gates and assures no further change in the master flip-flop. Below V_{T2}, the transfer gates are enabled, the slave and outputs are set according to information stored in the master. Below V_{T1}, the transfer gates are sure to be enabled under the worst case condition. The clock input reaches the ZERO level.

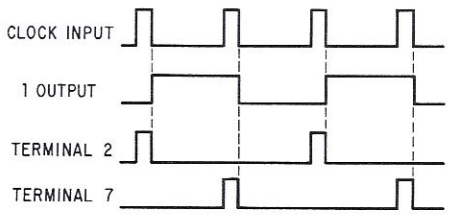
CLOCK INPUT VOLTAGE



Synchronous entry of information is done at the J and K inputs while the clock input is high.

Asynchronous information is entered at the S_D and C_D Direct Set and Direct Clear. A high level ONE is applied to the appropriate asynchronous input while the clock input is at the ZERO (low) level. Sufficient time must be allowed for the flip-flop to change state before the clock goes high.

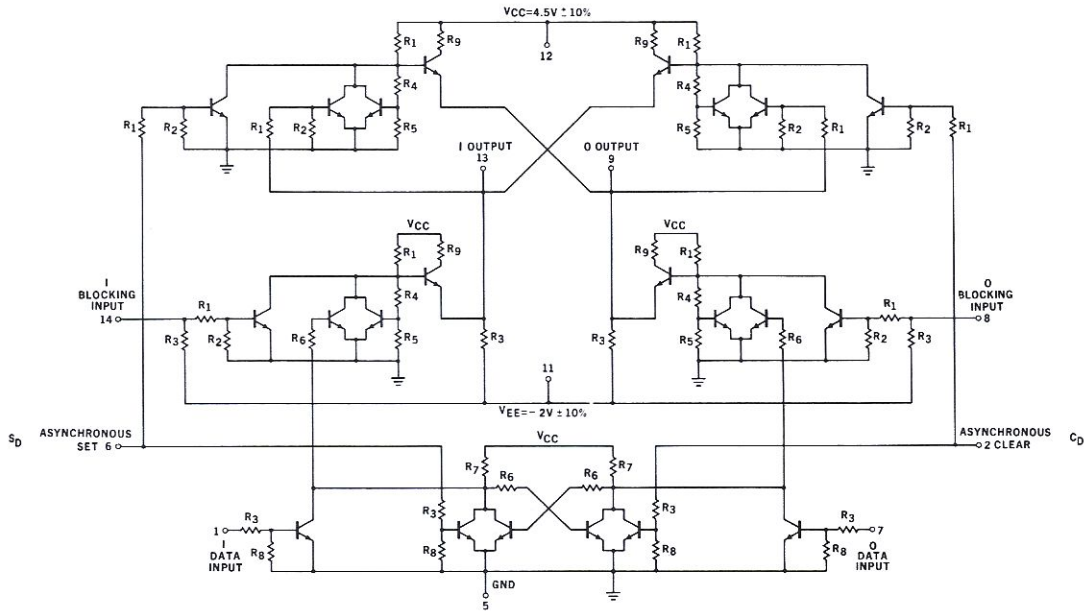
Pins 2 and 7 may serve as an output for a two phase clock having the same pulse duration as the clock input. Each output has a repetition rate of half the clock input frequency. (Fig. 1, Wired OR)



Pin 9, designated as a Logical Clear, may be used to block information from entering the J input without inhibiting the internal AND gate. It may also serve as an additional isolated J input.

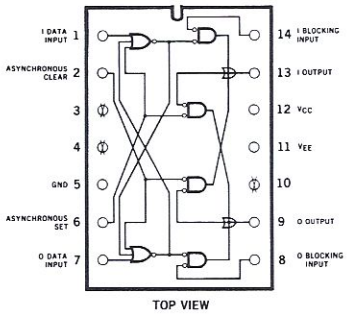
CTμL 9957 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



LOGIC DIAGRAM

(POSITIVE LOGIC)



TOP VIEW

TRUTH TABLE

S_n	C_n	Qnt + 1
0	0	Qn
0	1	0
1	0	1
1	1	Undetermined

NOTES:
(1) Connect pin 1 to pin 14 and pin 7 to pin 8
(2) Flip-Flop changes state on negative transition of input waveforms
(3) For asynchronous entry use pins 2 and 6

LOADING RULES

FLIP-FLOP UNITS	LOADING*
Data	1.0
SA, CA	2.0
Blocking	3.5
OUTPUTS	**FAN OUT**
Q, $\overline{Q}$	9.5

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	−4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

DC TESTS

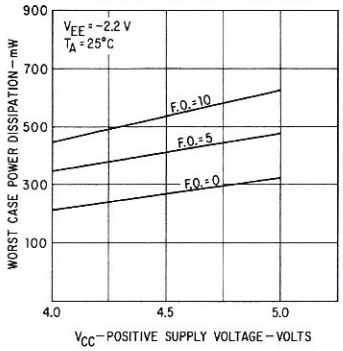
TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output			3.20 V	Volts	4.50	−2.00	No Load	Pulse note (1) to pin 3.
ONE Level Output	2.20			Volts	4.05	−2.20	[2]F.O. = 9.5	0.8 V to Pins 1 and 6, 2.5 V to Pin 8; Pulse to Pin 2. Guarantees min. ONE level output.
ONE Level Output	2.20			Volts	4.05	−2.20	F.O. = 9.5	2.5 V to Pins 2 and 6, 0.8 V to Pin 8.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 6, 1.25 V to Pin 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 2, 1.25 V to Pin 6, 2.5 V to Pin 14.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	1.25 V to Pin 8, 2.5 V to Pins 6 and 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	2.5 V to Pins 2, 8, 14; 1.25 V to Pin 13.
Input Current Data Input	1.5		2.25	mA	4.50	−2.0	No Load	2.5 V to Pins 1 and 7 sequentially.
Input Current Async. Input			6.75	mA	4.5	−2.0	No Load	2.5 V to Pins 2 and 6 sequentially. Guarantees asynchronous input loading.
Input Current Blocking Input			10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 8 and 14 sequentially.
Output Resistor	6.75		10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 6 and 9, Pins 2 and 13 sequentially.
Propagation Delay, t_{DR}		10	15	ns	4.5	−2.0	F.O. = 9.5	See Fig.
Propagation Delay, t_{DF}		17	30	ns	4.5	−2.0	F.O. = 9.5	See Fig.

NOTES:

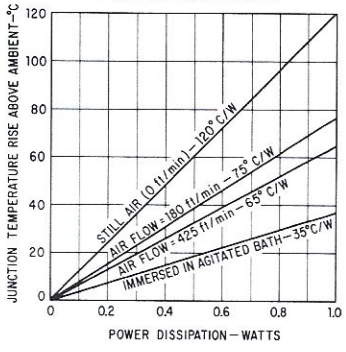
(1) Pulse, positive pulse of non-critical amplitude and width.
(2) F.O. = Fan-Out: F.O. = 9.5 equivalent to 168Ω to −2.20 V under worst case conditions.

ELECTRICAL CHARACTERISTICS

WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE

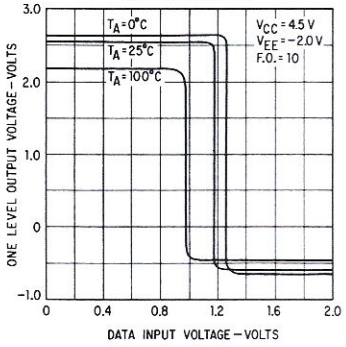


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

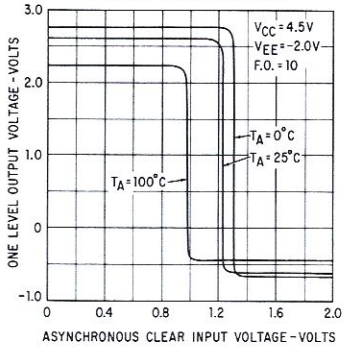


TRANSFER CHARACTERISTICS

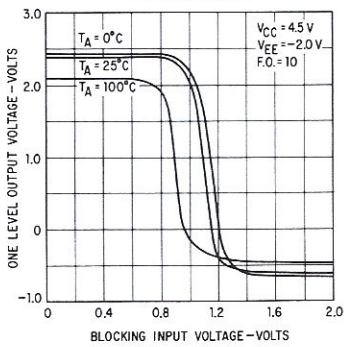
DATA INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE



ASYNCHRONOUS SET/CLEAR-ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

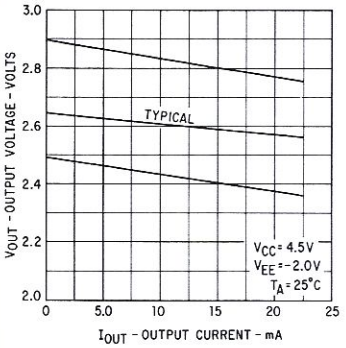


BLOCKING INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

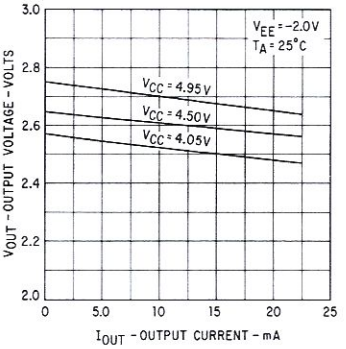


OUTPUT CHARACTERISTICS

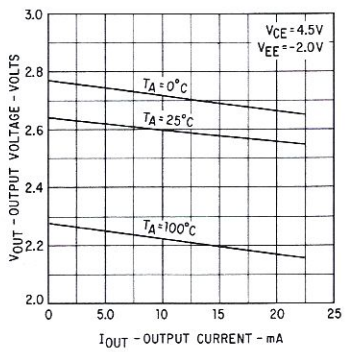
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

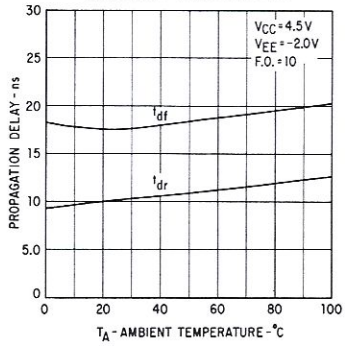


AS A FUNCTION OF TEMPERATURE

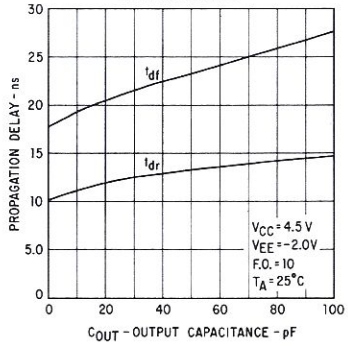


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

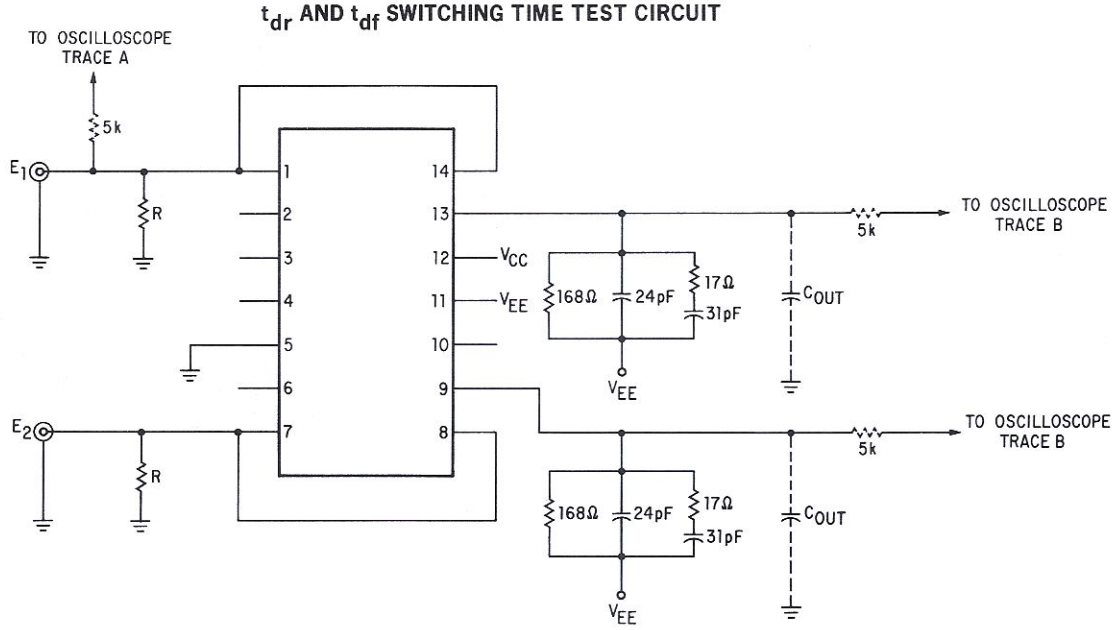


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

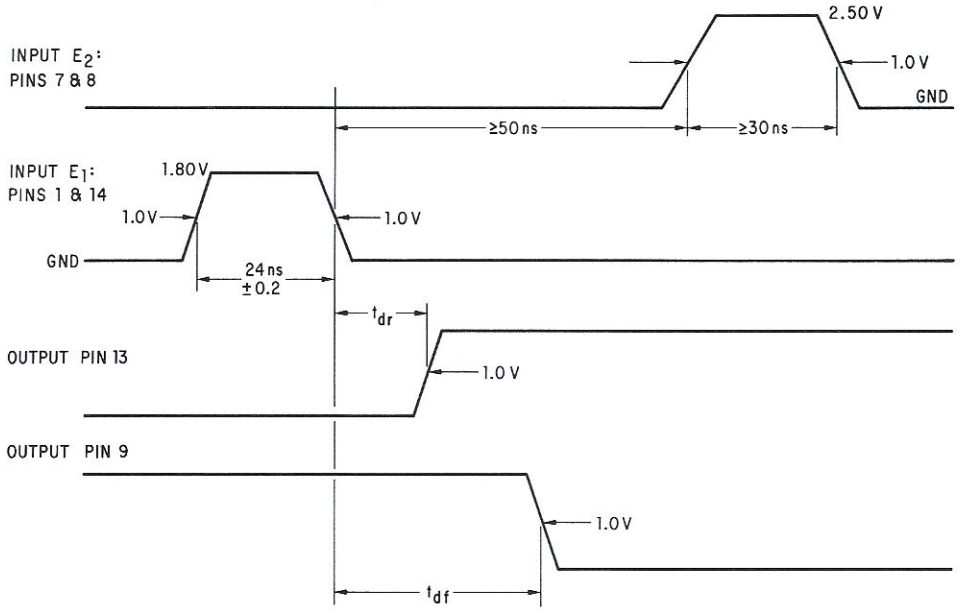


SWITCHING CHARACTERISTICS

t_{dr} AND t_{df} SWITCHING TIME TEST CIRCUIT



WAVEFORMS



SWITCHING NOTES:

(1) $V_{CC} = 4.50\ V \pm 10\%$
$V_{EE} = 2.00\ V \pm 10\%$
Select proper capacitor to provide adequate bypassing.

(2) Select R to provide proper termination for pulse generator used.

(3) Use oscilloscope with at least 5 k input impedance.

(4) Rise & Fall Times:
$t_f = t_r = 5ns$ measured at 10% to 90% points.

CTμL 9957 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

OPERATION OF FLIP-FLOP

The CTμL 9957 is a dual-rank directly-coupled R-S Flip-Flop. The first rank or "master" consists of two cross-coupled NOR gates similar to the CTμL 9952. The second rank or "slave" employs OR ties as shown in the functional logic diagram, thereby minimizing through delay. Two NAND gates provide feedback inversion, while the other two provide gating between "master" and "slave."

The primary data inputs to the Flip-Flop are through pins 1 and 7. These inputs work directly from AND gate outputs, allowing OR ties and multiple inputs to each Flip-Flop.

To take advantage of the dual-rank principle, mutually exclusive active inputs should be applied to the gating to "master" and "slave" so that only one or the other can change at any particular instant. This is easily accomplished in the CTμL 9957 due to the difference in active polarity of the two gates. Thus, what appears as a logic 1 to CTμL gates of the Flip-Flop data inputs is a logic 0 to the "slave" gates, and vice versa.

These observations lead to the connection of pin 1 to pin 14 and pin 7 to pin 8 as shown in Fig. 2. Although both "slave" gates are not necessarily inhibited when a change takes place, the output cannot change unless both data inputs are logic 0. Therefore, this connection is the usual one, tending to minimize the loading of timing circuits.

In case phased timing signals are advantageous, pins 8 and 14 may be used independently as long as they are never active (low) while their corresponding data inputs are high.

Direct inputs to both "master" and "slave" appear on pins 2 and 6. A logic (high) on either input sets or resets the "master" and simultaneously inhibits a feedback NAND gate in the "slave." The net effect is that both "master" and "slave" move to the desired condition during the presence of the direct input signal.

The response of the Flip-Flop to concurrent inputs tending to set opposite output conditions is ambiguous. That is, simultaneous logic 1 inputs must be avoided for well-defined operation.

APPLICATION

FIG. 1 DUAL RANK FLIP-FLOP CONNECTED FOR TWO-PHASE CLOCKING, J-K MODE

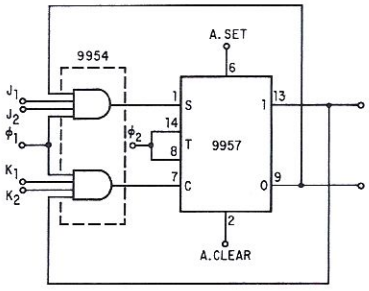


FIG. 2 DUAL RANK FLIP-FLOP CONNECTED FOR SINGLE-PHASE CLOCKING, J-K MODE

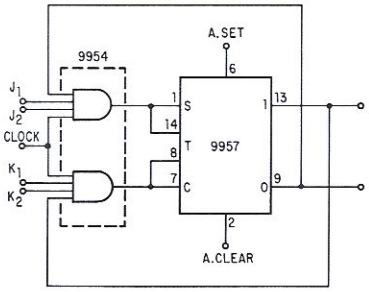


FIG. 3 SERIAL BINARY COUNTER

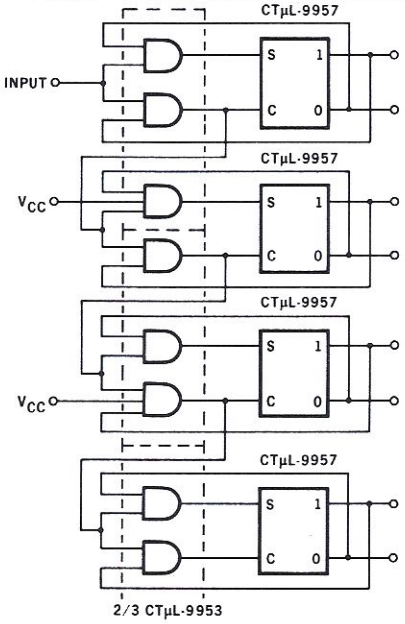
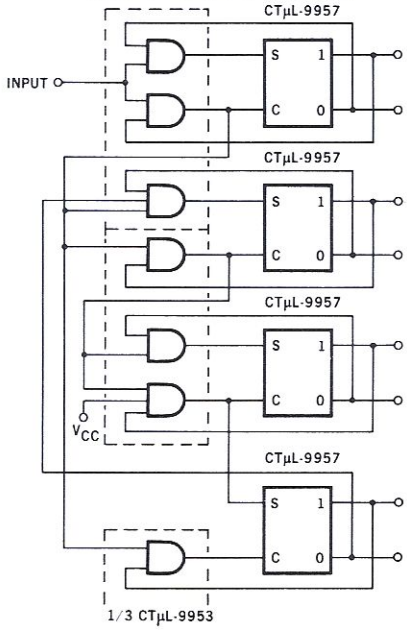


FIG. 4 1-2-4-8 DECADE



NOTES:
1. On all CTμL 9957's, tie pins 1-14 and 7-8.
2. All gates are CTμL 9953's.

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